IN THE SPECIFICATION:

Please amend paragraph number **[0001]** as follows:

[0001] This application is a divisional of application Serial No. 09/399,592, filed September 20, 1999, ~~pending.~~ now U.S. Patent 6,468,859, issued October 22, 2002.

Please amend paragraph number **[0020]** as follows:

[0020] Wafer 10 has been provided with an array of substantially electrically isolated word lines, such as the illustrated word lines 12, 14, and 16. Such word lines are of a conventional construction having a lowermost gate oxide, a lower polysilicon layer, an overlying silicide layer such as tungsten silicide, and insulating ~~caps~~ caps 18 and side insulating ~~spacers 18.~~ spacers. Such spacers and caps 18 preferably comprise an insulative nitride, such as Si_3N_4. A thin layer 20 of Si_3N_4 or TetraEthylOrthoSilicate (TEOS) is provided atop the wafer to function as a diffusion barrier for subsequent ~~BoroPhosoSilicate~~ BoroPhosphoSilicate Glass (BPSG) deposition. Layer 20 has a thickness preferably from about 100 Angstroms to about 250 Angstroms.

Please amend paragraph number **[0025]** as follows:

[0025] In accordance with the invention, buried capacitor contact openings/containers 38 and associated pillars 40 can be provided along with the bit line contact openings 32 and pillars 34, as seen in Figures 3 and 4. A first layer of electrically conductive material 36 is provided over insulating material layer 28 ~~to within~~ within first contact opening 38 and second contact opening 32 to electrically connect with first and second active regions 22, 26 and 24, respectively. First layer 36 is deposited to a thickness which fills first contact opening 38 and second contact opening 32. An example diameter for contact openings 32 and 38 is 0.2-0.25 micron. In such instance, an example preferred thickness of first layer 36 is less than 2,000 Angstroms, which is sufficient to fill the contact openings 32, 38. An example and preferred material for first layer 36 is in situ N+ doped polysilicon.

Please amend paragraph number **[0026]** as follows:

[0026] Wafer fragment 10 is planarized and etched downwardly at least to upper surface 30 of insulating ~~material~~ layer 28 to remove conductive material layer 36 thereabove. This will isolate first layer conductive material layer 36 within contact openings 32 and 38. Such planarized etching can be conducted by plasma etchback or by chemical-mechanical polishing.

Please amend paragraph number **[0027]** as follows:

[0027] Referring to Figure 5, the conductive material layer 36 within first contact opening 38 can be recessed further, to a level below upper surface 30 of insulating layer 28. A capacitor structure is formed at this location, as discussed below.

Please amend paragraph number **[0030]** as follows:

[0030] Referring to Figure 7, CMP is preferably used to remove the conductive material layer 58 which is disposed atop insulating layer 54, thereby defining isolated storage node containers 62 (see Figure 7). The storage node containers 62 are electrically connected to first active regions 22 and 26 through pillars 40.

Please amend paragraph number **[0032]** as follows:

[0032] A conductive capacitor cell layer 70, ~~such as~~ such as a cell plate, is provided atop the capacitor cell dielectric layer 68, thereby defining an array of memory cell capacitors 72 on the wafer 10. Individual memory cell capacitors, such as the illustrated capacitors 72, of the array are thus provided within the capacitor contact openings and are defined by an outwardly projecting container structure. Cell layer 70 preferably comprises in situ phosphorous-doped polysilicon and functions as a capacitor cell plate.

Please amend paragraph number **[0034]** as follows:

[0034] The etch of the cell layer 70 has an isotropic component, i.e., the etch proceeds in both horizontal and vertical directions at relatively the same rate. The polysilicon layer that

comprises cell layer 70 is selectively etchable with respect to the cell ~~nitride~~ dielectric layer 68. Hence, the cell ~~nitride~~ dielectric layer 68 is not etched at the same rate and an overetch of the cell layer 70 results in an undercut profile. One consequence of the undercut of cell layer 70 is that, with a worst case scenario, photolithography may result in a misalignment edge 73, as seen in Figure 9, wherein the cell layer 70 is isotropically etched back past the upper edge of the conductive material layer 58.

Please amend paragraph number **[0037]** as follows:

[0037] As shown in Figure 10, an electrically insulative layer 76, such as TEOS, is blanket deposited atop the wafer 10 (and, therefore, covers cell layer 70) to a thickness from about 150 Angstroms to about 1,500 Angstroms, preferably 500 Angstroms. The purpose of ~~such a~~ such an insulative layer 76 is to cover both the exposed corner of the conductive material layer 58 and any damaged cell ~~nitride~~ dielectric layer 68. Further, the blanket TEOS film or layer 76 is superior to the use of a nitride film as it also allows hydrogen to diffuse through it and, consequently, does not prevent passivation by hydrogen of the FETs during alloy.

Please amend paragraph number **[0038]** as follows:

[0038] Continuing the process flow, Figure 10 illustrates a layer of insulating material 78 overlying the electrically insulative layer 76 or barrier layer and underlying layers and ~~capacitor structures~~ memory cell capacitors 72. The layer of insulating material 78 is preferably comprised of ~~a BPSG layer 78.~~ BPSG. Alternatively, a deposited anti-reflective coating (not shown) may be added atop the BPSG insulating material layer 78 for increased photolithography resolution. The wafer 10 is coated with a layer of resist 79 and is patterned.

Please amend paragraph number **[0039]** as follows:

[0039] Preliminary bit line contact openings 80 are provided through overlying BPSG insulating material layer 78, TEOS insulative layer 76 and second BPSG insulating layer 54 down to the pillar 34. The anisotropic plasma etch used to produce contact opening 80 is

followed by a pre-metal clean, also known as a wet etch as oxide material is isotropically removed. The pre-metal clean/wet etch removes any anti-reflective coating (DARC) remaining on the top surface of the BPSG insulating material layer 78 and cleans the bottom of the contact opening 80.

Please amend paragraph number **[0040]** as follows:

[0040] Typically, the process incidentally would move out laterally when the wet etch process hits the cell ~~nitride~~ dielectric layer 68. However, the TEOS ~~film~~ insulative layer 76 deposited atop of the wafer 10 after the cell layer 70 has been etched serves to substantially eliminate any preferential wet etching along the seam of the cell ~~nitride~~ dielectric layer 68 and BPSG insulating material layer 78, which would occur if the TEOS insulative layer 76 had not been deposited.

Please amend paragraph number **[0041]** as follows:

[0041] Without the TEOS insulative layer 76, when the pre-metal clean/wet etch hits the cell ~~nitride~~ dielectric layer 68, an enhanced etch rate would occur along the interface with the BPSG insulating material layer 78. This enhanced etch rate is due to stress and dopant "pile-up" from the BPSG insulating material layer 78 and ~~out-diffusion~~ out-diffusion from the heavily doped exposed cell layer 70. Higher out-diffusion and higher phosphorous concentration from the exposed cell layer 70 leads to an enhanced wet etch rate. This will be exacerbated by subsequent wet cleans prior to contact metal deposition, which can ultimately lead to bit contact-to-cell layer 70 shorts.

Please amend paragraph number **[0042]** as follows:

[0042] The presence of the TEOS insulative layer 76 moves the stress away from the nitride/BPSG interface to the TEOS/BPSG interface. The result is that the cell layer 70 is no longer exposed during the pre-metal clean/wet etch. The TEOS ~~film~~ insulative layer 76 prevents dopant mixing or "pile up" (an increase in the concentration of dopants in a particular location).

Thus, the TEOS insulative layer 76 provides a stress buffer and dopant barrier in the form of a TEOS film that is deposited after the capacitor cell ~~plate~~ layer 70 is etched and cleaned.

Please amend paragraph number **[0043]** as follows:

[0043] The addition of a TEOS ~~film~~ insulative layer 76 buffers the stress as well as eliminates dopant mixing between the highly phosphorous doped polycrystalline silicon forming the capacitor cell layer 70 and the heavily doped BPSG insulating material layer 78 and, therefore, provides a method of reducing stress-induced wet etching along the BPSG/nitride interface in a DRAM capacitor to eliminate bit contact-to-cell layer 70 shorting.